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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,145	10/02/2001	Nick A. Youker	279.361US1	9584

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,145	YOUKER ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-02-01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group II, claims 7-13 and 20-25, in Paper No. 3 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

A. Claim 7 recites the limitations "a circuit board; an IC chip connected to the circuit board" and "an electrical component mounted on or above a surface of the IC chip".

However, Fig. 3 does not show the chip being connected to the circuit board.

B. Claim 11 recites the limitations "a circuit board", "a TAB leadframe connecting the IC chip to the circuit board" and "an electrical component mounted on or above the major surface of the IC chip".

However, Fig. 3 or 5 does not show the leadframe connecting the chip to the board such that the electrical component is mounted on/above the major surface of the IC chip".

Therefore, the must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 9, 11, 12, 20-22, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US Pat. 5892271) in view of Bickford et al. (US Pat. 4862322).

Regarding claims 7, 9 and 20-22, Takeda et al. teach an electrical device comprising:

- a tape automated bonding (TAB) leadframe (TABLF) substrate (see 4 in Fig. 3 and 10), the TABLF being made of a flexible polyimide/tape material (Col. 3, line 66)
- the TABLF including a plurality of leads (see 8 in Fig. 3 and 10), the leads having a first area of the plurality of leads being internally routed and configured into an inner lead bonding (ILB) area/portion and an outer lead bonding (OLB) area/portion having external electrodes (see 6 in Fig. 3; Col. 4, line 7))
- an integrated circuit (IC) chip (1 in Fig. 3) being connected to an exposed portion of the lead in the ILB portion of the TABLF
- the first area of the plurality of leads being dimensioned to directly connect one or more of the plurality of leads to the perimeter electrodes/I-O pads of the IC chip, the ILB portion of the leads having terminals/contacts being exposed (see 7 in the ILB portion under the IC chip in Fig. 3), and
- the IC chip having bonding pads/input-output (I/O) connections at a perimeter of the chip

(Fig. 3 and 10; Col. 3, line 50- Col. 4, line 40).

Takeda et al. fail to teach :

- the chip being connected to a circuit board by the TABLF through the leads in the OLB portion, and
- an electrical component mounted on or above a surface of the IC chip and electrically connected to the IC chip via the lead, which extends from the electrical component to the IC chip.

Bickford et al. teach a TABLF having a plurality of electrical components/chips (see 76 and 36 Fig. 15 and 2 respectively), the TABLF comprising:

- an IC chip being connected to a printed circuit board (PCB) by the TABLF (see 80 and 212 respectively in Fig. 15) through a bonding pad (216 in Fig. 15) in an OLB portion (102/98 in Fig. 15) of leads
- an electrical component/second chip (78 in Fig. 15; Col. 9, line 35) being mounted on the IC chip and being electrically connected to the IC chip via an exposed ILB portion (see 94/100 in Fig. 15) which extends from the electrical component to the perimeter bonding pads/input-output (I/O) connections of the IC chip, and
- the ILB and the OLB having generally rectangular shapes (see the 38 and 40 in Fig. 2)

(Fig. 2 and 15; Col. 8, lines 1-45; Col. 17, line 60- Col. 18, line 34).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chip being connected to a circuit board by the TABLF and the electrical component mounted on or above a surface of the IC chip and electrically connected to the IC chip via the lead which extends from the electrical component to the IC as taught by Bickford et al. so that the desired multilevel connection and circuit integration with the PCB can be achieved in Takeda's TABLF.

Regarding claims 11, 12, 22, 24 and 25, Takeda et al. and Bickford et al. teach substantially the entire claimed structure as applied to claim 7 above.

5. Claims 8 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US Pat. 5892271) and Bickford et al. (US Pat. 4862322) as applied to claim 7 above, and further in view of Buckley, III et al. (US Pat. 5477082).

Regarding claim 8, Takeda et al. teach substantially the entire claimed structure as applied to claim 7 above, wherein Takeda et al. teach the TABLF having external terminals (see 7 in Fig. 3) to provide an electrical connection to the chip via the leads (see 8 in Fig. 3), but fail to teach using at least two electrical components being are mounted on/above the surface of the IC chip and each being electrically connected to the IC chip via leads on the TABLF which extend from each of the electrical components to perimeter I/O of the IC chip.

Buckley, III et al. teach a bi-planar multichip module (MCM- see Fig. 6 and 7) having a flexible carrier/TABLF (60 in Fig. 6) where two or more electrical components/chips (see 58A, 90, etc. in Fig. 6 and 7) are mounted above a first IC chip (see 56 in Fig. 6) the surface of the IC chip and each being electrically connected to the IC chip via respective traces/leads and vias (see 24A in Fig. 3 and 6) on the TABLF, which extend from each of the electrical components to perimeter pads/I/O contacts/bumps of the first IC chip (Fig. 3, 6 and 7; Col. 2, lines 3-25; Col. 3, lines 30-54; Col. 7, lines 55- 67).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate using at least two electrical components being are mounted on/above the surface of the IC chip and each being electrically connected to the IC chip via leads on the TABLF which extend from each of the electrical components to perimeter I/O of the IC chip as taught by Buckley, III et al. so that the desired multilevel connection and an improvement in the chip density can be achieved in Bickford et al. and Takeda's TABLF.

6. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US Pat. 5892271) and Bickford et al. (US Pat. 4862322) as applied to claim 7 above, and further in view of admitted prior art (APA).

Regarding claims 10 and 13, Takeda et al. teach substantially the entire claimed structure as applied to claims 7 and 11 above, except the IC chip being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device is dimensioned to be implantable within a body.

The APA teaches using conventional TABLF devices being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device being implantable within a body (see specification pages 1 and 2). Furthermore, determination of parameters including dimensions such as length/width, size, etc., and weight of a TAB device in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired effect/result for particular applications including medical, military, communication, etc.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC chip being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device is dimensioned to be implantable within a body as taught by the APA so that the desired benefits and reliability of the device for the medical application can be achieved in Bickford et al. and Takeda's TABLF.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

09-15-04

NITIN PAREKH

PATENT EXAMINER

Technology Center 2800